

WHAT IS CLAIMED IS:

1 1. A method of isolating a trench, comprising:
2 forming a first trench and a second trench in a first region
3 and a second region of a semiconductor substrate, respectively;
4 forming a lower isolation pattern to fill a lower region of the
5 first trench; and
6 forming an upper isolation pattern to fill an upper region of
7 the first trench and the second trench.

1 2. The method as claimed in claim 1, wherein the
2 second trench is formed to be wider than the first trench.

1 3. The method as claimed in claim 1, wherein the first
2 and second regions are a cell array region and a peripheral circuit
3 region, respectively.

1 4. The method as claimed in claim 1, wherein forming
2 the first and second trenches comprises:
3 forming a pad oxide pattern and a polish stop pattern which
4 are sequentially stacked on the semiconductor substrate; and
5 etching the semiconductor substrate using the polish stop
6 pattern as an etch mask.

1 5. The method as claimed in claim 1, wherein forming
2 the lower isolation pattern comprises:

3 forming a lower isolation layer on an entire surface of the
4 semiconductor substrate where the first and second trenches are
5 formed;

6 forming a photoresist pattern on the first region of the
7 semiconductor substrate having the lower isolation layer formed
8 thereon, leaving the second region exposed;

9 etching the lower isolation layer in the second region using
10 the photoresist pattern as an etch mask to expose at least an
11 upper sidewall of the second trench;

12 removing the photoresist pattern; and

13 etching the lower isolation layer remaining on a resultant
14 structure where the photoresist pattern is removed, to expose an
15 upper sidewall of the first trench and simultaneously to form a
16 lower isolation pattern for filling a lower region of the first trench.

1 6. The method as claimed in claim 5, wherein the lower
2 isolation layer is formed of a spin on glass (SOG) layer.

1 7. The method as claimed in claim 5, wherein the
2 etching of the lower isolation layer is performed using a dry etch, a
3 wet etch, or a mixture of both.

1 8. The method as claimed in claim 7, wherein the etching
2 of the lower isolation layer is performed using a wet etch including
3 a fluoric acid as an etchant.

1 9. The method as claimed in claim 1, wherein the forming
2 of the lower isolation pattern comprises:

3 forming a lower isolation layer on an entire surface of the
4 semiconductor substrate where the first and second trenches are
5 formed;

6 etching the lower isolation layer to form a lower isolation
7 pattern in a lower region of the first trench;

8 forming a photoresist pattern on the first region of the
9 semiconductor substrate having the lower isolation pattern formed
10 thereon, leaving the second region exposed;

11 removing the lower isolation layer remaining in the second
12 region using the photoresist pattern as an etch mask; and

13 removing the photoresist pattern.

1 10. The method as claimed in claim 9, wherein the lower
2 isolation layer is formed of an SOG layer.

1 11. The method as claimed in claim 9, wherein etching the
2 lower isolation layer is performed using a wet etch, a dry etch or a
3 mixture of both.

1 12. The method as claimed in claim 1, wherein forming the
2 upper isolation pattern comprises:

3 forming an upper isolation layer on an entire surface of the
4 semiconductor substrate that results after forming the lower
5 isolation pattern; and

6 planarizing the upper isolation layer to expose a top surface
7 of the semiconductor substrate.

1 13. The method as claimed in claim 12, wherein
2 planarizing the upper isolation layer is performed using a chemical
3 mechanical polishing (CMP) process.

1 14. The method as claimed in claim 1, after forming the
2 first and second trenches, further comprising forming a nitride liner
3 on the entire surface of the semiconductor substrate comprising
4 the first and second trenches.

1 15. The method as claimed in claim 14, wherein the nitride
2 liner is formed of a low-pressure chemical vapor deposition
3 (LPCVD) silicon nitride layer.

1 16. The method as claimed in claim 15, wherein the nitride
2 liner is conformally formed to a thickness of from about 30 to
3 140 Å.

1 17. The method as claimed in claim 1, wherein the upper
2 isolation pattern is formed of at least one of a high-density plasma
3 (HDP) oxide layer and a USG layer.

1 18. The method as claimed in claim 17, wherein when the
2 upper isolation pattern is formed of an HDP oxide layer, an LPCVD
3 oxide layer is formed on the substrate including the nitride liner
4 before forming the HDP oxide layer.

1 19. The method as claimed in claim 18, wherein the
2 LPCVD oxide layer is formed to a thickness of about 100 Å.

1 20. The method as claimed in claim 1, after forming the
2 lower isolation pattern, further comprising performing a thermal
3 oxidizing process to densify the lower isolation pattern.

1 21. The method as claimed in claim 20, wherein the
2 thermal oxidizing process is a curing process.

1 22. The method as claimed in claim 21, wherein the curing
2 process uses oxygen gas or deionized water.

1 23. A structure of trench isolation, comprising:
2 a first trench and a second trench that are formed in a first
3 region and a second region of a semiconductor substrate,
4 respectively;
5 a lower isolation pattern filling a lower region of the first
6 trench while exposing an upper sidewall of the first trench; and
7 an upper isolation pattern filling the second trench and an
8 upper region of the first trench.

1 24. The structure as claimed in claim 23, further
2 comprising a nitride liner pattern to cover inner walls of the first
3 and second trenches.

1 25. The structure as claimed in claim 24, wherein the
2 nitride liner is silicon nitride.

1 26. The structure as claimed in claim 25, wherein the
2 nitride liner is formed by low pressure chemical vapor deposition
3 (LPCVD).

1 27. The structure as claimed in claim 25, wherein the
2 nitride liner is formed to a thickness of about 30 to 140 Å.

1 28. The structure as claimed in claim 23, wherein the
2 lower isolation pattern is formed of an SOG layer.

1 29. The structure as claimed in claim 23, wherein the
2 upper isolation pattern is formed of at least one of an HDP oxide
3 layer and a USG layer.

1 30. The structure as claimed in claim 29, wherein when
2 the upper isolation pattern is formed of an HDP oxide layer, an
3 LPCVD oxide layer is formed on the substrate including the nitride
4 liner before forming the HDP oxide layer.

1 31. The structure as claimed in claim 30, wherein the
2 LPCVD oxide layer is formed to a thickness of about 100 Å.